Specification

Applicants have herein amended the Summary section of the Specification to conform to the claims of the instant application.

Claims

Claims 17, 29, 125, and 128 have been amended. Claims 113, 118, 121, 124, and 127 have been canceled.

Claims 17, 19, 29, 30, 98-111, 114-116, 119-120, 122-125, and 128

In the Office Action, the Examiner rejected claims 17, 19, 29, 30, 98-111, 114-116, 119-120, 122-125, and 128 under 35 U.S.C. §102(e) as anticipated by U.S. Patent No. 5,977,561 ("Wu"). Applicants traverse the rejection as follows.

Under 35 U.S.C. §102(e), a claim is anticipated only if each and every element as set forth in the claim is found in a prior art reference. *See* MPEP §2131. Applicants submit that the Office has not established that Wu anticipates the present application because not all elements of claims 17, 29, 125, and 128, as amended, are found in the cited reference.

Wu is directed to a boron-doped glass spacer that is located on each sidewall of the gate and functions as both an insulator and a source/drain junction diffusion source. *See* Wu, col. 4, lines 34-38; col. 4, lines 62-65; col. 5, lines 49-51. Applicants submit that the spacer in Wu contributes to the performance of the device disclosed in Wu, in that the spacer is used not only to insulate the gate from the source and drain, but also to diffuse a boron dopant, a function that could not be accomplished if the spacer was replaced with an air gap, as disclosed in the present application. Thus, replacing the boron-doped spacer with an air gap, as disclosed in the present application, would destroy the intended function of the design disclosed in Wu. Therefore,

Applicants submit that Wu does not disclose, among other things, an air gap as claimed in claims 17, 29, 125, and 128.

In addition, Wu does not disclose, among other things, a location and structure of a gap, as claimed in claims 17, 29, 125, and 128, that not only insulates the gate from the source and drain but also enables shallow junctions to be separate from, but in communication with, the source and drain. Furthermore, Wu does not disclose, among other things, a location and structure of a gap, as claimed in claims 17, 29, 125, and 128, that enables the shallow junctions to be implanted with a dopant that is oppositely charged from that of the source and drain.

Thus, Applicants submit that claims 17, 29, 125, and 128 are not anticipated by Wu because Wu does not disclose each and every element of the claims, and thus, claims 19, 98-103, which depend from claim 17, and claims 30, 104-112, 114-117, 119-120, 122-123, which depend from claim 29, are not anticipated by Wu for the same reasons stated hereinabove.

Claims 29, 110-112, 115-117, 125, and 126

In the Office Action, the Examiner rejected claims 29, 110-112, 115-117, 125 and 126 under 35 U.S.C. §102(b) as anticipated by Moravvej-Farshi et al. M. K. Moravvej-Farshi and M. A. Green, *Novel Self-Aligned Polysilicon-Gate MOSFETs with Polysilicon Source and Drain*, 30 SOLID-STATE ELECTRONICS 1053 (1987) ("Moravvej"). Applicants traverse the rejection as follows.

Under 35 U.S.C. §102(b), a claim is anticipated only if each and every element as set forth in the claim is found in a prior art reference. *See* MPEP §2131. Applicants submit that the Office has not established that Moravvej anticipates the present application because not all elements of claims 29 and 125, as amended, are found in the cited reference.

Moravvej is directed to a masking oxide sequence that self-aligns the gate between the source and the drain. *See* Moravvej, supra, at 1053, 1058. Moravvej states that "[e]tching of the second polysilicon layer in regions not protected by the oxide until the oxide of the first polysilicon layer is exposed will leave the top layer of polysilicon perfectly aligned to the original source and drain regions of the transistor..." Moravvej, supra, at 1054. In addition, Moravvej utilizes silicon dioxide both to achieve this self-aligning process and to insulate the gate from the drain and source. *See* Moravvej, supra, at 1054.

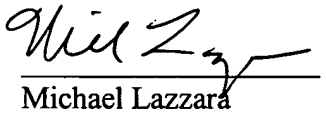
However, Applicants submit that Moravvej does not disclose, among other things, a location and structure of a gap, as claimed in claims 29 and 125, that not only insulates the gate from the source and drain but also enables shallow junctions to be separate from, but in communication with, the source and drain. Furthermore, Moravvej does not disclose, among other things, a location and structure of a gap, as claimed in claims 29 and 125, that enables the shallow junctions to be implanted with a dopant that is oppositely charged from that of the source and drain.

Thus, Applicants submit that claims 29 and 125 are not anticipated by Moravvej because Moravvej does not disclose each and every element of the claims, and thus, claims 30, 104-112, 114-117, 119-120, 122-123, which depend from claim 29, and claim 126, which depends from claim 125 are not anticipated by Moravvej for the same reasons stated hereinabove.

CONCLUSION

Applicants respectfully request a Notice of Allowance for the pending claims in this application. If the Examiner is of the opinion that the instant application is in condition for disposition other than allowance, the Examiner is respectfully requested to contact Applicants' attorney at the telephone number listed below in order that the Examiner's concerns may be expeditiously addressed.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims

The claims have been amended as follows:

17. (Amended) A transistor formed on a substrate assembly, comprising:

[a gate structure;]

a raised drain structure;

a raised source structure;

a gate located between said source and said drain;

a first capping layer in communication with at least a portion of said gate and said source;

a first portion of a gate oxide region in communication with at least a portion of said gate and said source;

said source, said gate, said first capping layer, and said first portion of said gate oxide region defining a first gap therein, said first gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said first gap and any one of said gate, said source, said first capping layer, and said first portion of said gate oxide region;

a first implant junction area located in a substrate assembly beneath said first gap and extending partially beneath said gate and said source;

a second capping layer in communication with at least a portion of said gate and said drain;

a second portion of a gate oxide region in communication with at least a portion of said gate and said drain;

said drain, said gate, said second capping layer, and said second portion of said gate oxide region defining a second gap therein, said second gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said second gap and any one of said gate, said drain, said second capping layer, and said second portion of said gate oxide region; and

a second implant junction area located in a substrate assembly beneath said second gap and extending partially beneath said gate and said drain.

[a first junction area in the substrate assembly between said gate structure and said raised drain structure, said first junction area extending beneath said gate structure and said raised drain structure; and]

[a second junction area in the substrate assembly between said gate structure and said raised source structure, said second junction extending beneath said gate structure and said raised source structure.]

29. (Amended) A transistor, comprising:

[a gate structure;]

a raised drain structure;

a raised source structure;

a gate located between said source and said drain;

a first capping layer in communication with at least a portion of said gate and said source;

a first portion of a gate oxide region in communication with at least a portion of said gate and said source;

said source, said gate, said first capping layer, and said first portion of said gate oxide region defining a first gap therein, said first gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said first gap and any one of said gate, said source, said first capping layer, and said first portion of said gate oxide region;

a first implant junction area located in a substrate assembly beneath said first gap and extending partially beneath said gate and said source;

a second capping layer in communication with at least a portion of said gate and said drain;

a second portion of a gate oxide region in communication with at least a portion of said gate and said drain;

said drain, said gate, said second capping layer, and said second portion of said gate oxide region defining a second gap therein, said second gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said second gap and any one of said gate, said drain, said second capping layer, and said second portion of said gate oxide region;

a second implant junction area located in a substrate assembly beneath said second gap and extending partially beneath said gate and said drain;

first means for providing a conductive path between said gate structure and said raised drain structure; and

second means for providing a conductive path between said gate structure and said raised source structure.

125. (Amended) A transistor formed on a substrate assembly, comprising:

[a gate structure;]

a raised drain structure;

a raised source structure;

a gate located between said source and said drain;

a first capping layer in communication with at least a portion of said gate and said source;

a first portion of a gate oxide region in communication with at least a portion of said gate and said source;

said source, said gate, said first capping layer, and said first portion of said gate oxide region defining a first gap therein, said first gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said first gap and any one of said gate, said source, said first capping layer, and said first portion of said gate oxide region;

a first implant junction area located in a substrate assembly beneath said first gap and extending partially beneath said gate and said source, wherein said first junction area includes doped silicon areas;

a second capping layer in communication with at least a portion of said gate and said drain;

a second portion of a gate oxide region in communication with at least a portion of said gate and said drain;

said drain, said gate, said second capping layer, and said second portion of said gate oxide region defining a second gap therein, said second gap having one of a gas and

a vacuum therein, wherein no dielectric material is positioned between said second gap and any one of said gate, said drain, said second capping layer, and said second portion of said gate oxide region; and

a second implant junction area located in a substrate assembly beneath said second gap and extending partially beneath said gate and said drain, wherein said second junction area includes doped silicon areas.

[a first junction area in the substrate assembly between said gate structure and said raised drain structure, said first junction area extending beneath said gate structure and said raised drain structure; and]

[a second junction area in the substrate assembly between said gate structure and said raised source structure, said second junction extending beneath said gate structure and raised source structure, wherein said first and second junction areas include doped silicon areas.]

128. (Amended) A transistor formed on a substrate assembly, comprising:

[a gate structure;]

a raised drain structure;

a raised source structure;

a gate located between said source and said drain;

a first capping layer in communication with at least a portion of said gate and said source;

a first portion of a gate oxide region in communication with at least a portion of said gate and said source;

said source, said gate, said first capping layer, and said first portion of said gate oxide region defining a first gap therein, said first gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said first gap and any one of said gate, said source, said first capping layer, and said first portion of said gate oxide region;

a first implant junction area located in a substrate assembly beneath said first gap and extending partially beneath said gate and said source, wherein said first junction area includes a pocket implant junction;

a second capping layer in communication with at least a portion of said gate and said drain;

a second portion of a gate oxide region in communication with at least a portion of said gate and said drain;

said drain, said gate, said second capping layer, and said second portion of said gate oxide region defining a second gap therein, said second gap having one of a gas and a vacuum therein, wherein no dielectric material is positioned between said second gap and any one of said gate, said drain, said second capping layer, and said second portion of said gate oxide region; and

a second implant junction area located in a substrate assembly beneath said second gap and extending partially beneath said gate and said drain, wherein said second junction area includes a pocket implant junction.

[a first junction area in the substrate assembly between said gate structure and said raised drain structure, said first junction area extending beneath said gate structure and said raised drain structure; and]

[a second junction area in the substrate assembly between said gate structure and said raised source structure, said second junction extending beneath said gate structure and raised source structure; and]

[wherein said first and second junction areas include pocket implant junctions.]

In the Specification

Paragraph at page 2, lines 6-9:

[The present invention is directed to a semiconductor structure which includes a raised source and a raised drain. The structure also includes a gate located between the source and drains. The gate defines a first gap between the gate and the source and a second gap between the gate and the drain.]

The present invention is directed to a transistor structure which includes a raised source, a raised drain, a gate located between the source and the drain, a first capping layer in communication with at least a portion of the gate and the source, a second capping layer in communication with at least a portion of the gate and the drain, a first portion of a gate oxide region in communication with at least a portion of the gate and the source, a second portion of a gate oxide region in communication with at least a portion of the gate and the drain. The source, the gate, the first capping layer, and the first portion of a gate oxide region define a first gap. The drain, the gate, the second capping layer, and the second portion of a gate oxide region define a second gap. The structure also includes a first junction area located beneath the first gap, the

gate and the source and a second junction area located beneath the second gap, the gate and the drain.

In the Abstract

[A semiconductor structure which includes a raised source and a raised drain. The structure also includes a gate located between the source and drains. The gate defines a first gap between the gate and the source and a second gap between the gate and the drain.]

A transistor structure which includes a raised source, a raised drain, a gate located between the source and the drain, a first capping layer in communication with at least a portion of the gate and the source, a second capping layer in communication with at least a portion of the gate and the drain, a first portion of a gate oxide region in communication with at least a portion of the gate and the source, a second portion of a gate oxide region in communication with at least a portion of the gate and the drain. The source, the gate, the first capping layer, and the first portion of a gate oxide region define a first gap. The drain, the gate, the second capping layer, and the second portion of a gate oxide region define a second gap. The structure also includes a first junction area located beneath the first gap, the gate and the source and a second junction area located beneath the second gap, the gate and the drain.